METHOD AND APPARATUS TO SEPARATE FIELD AND GRID PARAMETERS ON FIRST LEVEL WAFERS

DESCRIPTION

Background of Invention

[Para 1] Field of the Invention

[Para 2] This invention generally relates to photolithography, and more specifically, the invention relates to methods and systems for determining grid offsets for a photolithographic tool.

[Para 3] Background Art

[Para 4] Step-and-expose and step-and-scan photolithography tools (referred to as "steppers") are used extensively in the manufacture of large scale integrated circuits. A principal advantage of the use of steppers for the manufacture of integrated circuits is the ability of steppers to rapidly produce very fine patterns on the resist coated wafers.

[Para 5] In use, the stepper patterns wafers by producing a plurality of essentially identical fields that are placed adjacent to each other. The area of the wafer to be patterned is placed under the objective lens of the stepper and the field is exposed. The stepper then moves the wafer stage to the next portion of the wafer to be exposed. This process continues until all areas of the wafer requiring patterning have been exposed.

[Para 6] As integrated circuits require many levels of layers that must be properly placed relative to one another, steppers include an alignment system to aid in achieving the proper relative placement of the current level to the prior level or levels. However, the very first level to be printed on the wafer does not have access to alignment marks and this first level is exposed

without the use of the alignment system. This first level exposure process without the aid of the alignment system is sometimes referred to as "blind stepping."The first level exposure of multiple copies of identical fields can be modified by standard stepper systematic parameters. These include the field systematic parameters of field x magnification, field y magnification, field rotation, and field orthogonality. The first level exposure includes grid parameters of grid x magnification, grid y magnification, grid rotation and grid orthogonality.

[Para 7] In order to insure optimum overlay for subsequent levels, it is critical that the first level be exposed with known placement characteristics. To achieve these optimum results, it is essential that the field systematic parameters match the associated grid parameters. Also, when the stepper parameters that are applied at run-time are determined using feedback from lots previously exposed, it is important that the first level placement characteristics be consistent from lot to lot and preferably match the stepper baseline characteristics.

Summary of Invention

[Para 8] An object of this invention is to improve methods and systems for calibrating systematic grid parameters for a photolithographic tool.

[Para 9] Another object of the invention is to allow grid terms, in a photolithography procedure, to be measured independently of field terms.

[Para 10] A further object of the invention is to provide a stepper photolithography tool in which first level placement characteristics are consistent from lot to lot.

[Para 11] These and other objectives are attained with a method and system for calibrating grid parameters for a photolithographic tool. One embodiment of the invention utilizes artifacts located on the wafer stage. The artifacts are located outside of the area where a substrate would be placed. Typically, four artifacts are used, with two artifacts located along the same axis. The stage

moves a first artifact to the alignment system and the system measures the location of the first artifact. The stage then moves the second artifact, which is on the same axis but on the other side of the wafer stage, under the alignment system and measures the location of the second artifact.

[Para 12] This is repeated for the other two artifacts that line up in a second axis (i.e., perpendicular to the first axis). Grid offsets are calculated to provide, for example, grid magnification and rotation calibrations.

[Para 13] The preferred embodiments of the invention, described below in detail, have a number of advantages. For example, the invention allows grid terms to be measured independently of field terms, and when combined with the current practice, the invention allows the calculation of separate field errors and grid errors. In addition, the present invention does not require a separate photo level. Because of this, the invention reduces the cost of the product and, also, is not based on an assumption that the tool that laid down the photo, or zero, level, had no grid errors.

[Para 14] Further benefits and advantages of the invention will become apparent from a consideration of the following detailed description, given with reference to the accompanying drawings, which specify and show preferred embodiments of the invention.

Brief Description of Drawings

[Para 15] Figure 1 schematically illustrates a photolithography system that may be used in the practice of this invention.

[Para 16] Figure 2 is a top view of a waver having multiple exposure fields.

[Para 17] Figures 3 and 4 illustrate an existing procedure for measuring the difference between field and grid parameters in the photolithography system of Figure 1.

[Para 18] Figure 5 shows a first embodiment of the present invention.

[Para 19] Figure 6 illustrates a second embodiment of the invention.

[Para 20] Figure 7 depicts a third embodiment of this invention.

Detailed Description

[Para 21] The preferred embodiment of the invention applies to step-and-repeat or step-and-scan photolithography tools such as tool 10 shown in Figure 1. Photolithography tool 10 includes laser interferometer 12, which controls wafer stage 14. Tool 10 also includes alignment systems 16a, 16b, 16c and computer 18 to analyze alignment data. A substrate, such as silicon wafer 20, coated with photosensitive layer 22 is located on wafer stage 14.

[Para 22] With reference to Figure 2, in standard practice, step-and-repeat or step-and-scan photolithography tools place exposure fields 30a, 30b...30i on wafer 20 in an array pattern 32. In this operation, each alignment system 16a, 16b, 16c shines incident light beam 34 from a light source on wafer 20. The different alignment systems may be used either sequentially or in parallel, and data is collected for each alignment system.

[Para 23] As mentioned above, the first level of patterns to be printed on the wafer 20 does not have access to conventional alignment marks; and in order to form that first level, instrument parameters, referred to as field and grid parameters, are used. Today, through the use of overlapping metrology image, the difference between field and grid terms can be determined, however, grid terms cannot be separated from the field terms. As a result, adjustments to systematic errors are made based on the assumption that the grid terms are not fluctuating and that all variability seen is a result of fluctuations in field terms.

[Para 24] Figures 3 and 4 illustrate an existing procedure for measuring the difference between field and grid parameters. In this current practice, to get both field and grid parameters, the first level pattern forms measurable overlay structures 60 and 62 as fields are stepped across the wafer 20. This existing

practice may be continued, in combination with the preferred implementations of the present invention, to gather field-to-grid data.

[Para 25] The present invention provides methods and systems to independently measure grid parameters. Generally, the invention requires the use of two to four artifacts on the wafer stage, surrounding the wafer chuck. The wafer stage should preferably be made of a material that has zero coefficient of thermal expansion.

[Para 26] Figure 5 illustrates a first embodiment of the invention. At some frequency, whether before exposing the lot or each wafer, the wafer stage moves one stage artifact 66 to the alignment system, and the system measures the location of the artifact. The stage 14 now moves the artifact 70 that is in the same axis but on the other side of the wafer chuck, under the alignment system, and this system measures the location of this artifact 70.

[Para 27] This process is repeated for the two artifacts 72 and 74 that line up in the opposite axis. Since the physical distance between each artifact of a pair is known, the difference between the distance as measured by the interferometer of system and the known distance, provides grid magnification and rotation calibrations. These calibration factors can now be introduced while the first level wafers are being stepped.

[Para 28] Figure 6 illustrates a second embodiment of the invention. This embodiment may be used with one or more wafers. The wafer stage is moved so that one artifact 66 is under the alignment system, and the location of the artifact is measured. Next, the wafer stage 14 is moved a predetermined distance, and one-half 76 of a complete overlay metrology structure is exposed. The wafer stage is moved so that the other artifact 70 in the same axis is under the alignment system, and the location of this artifact is measured. Now, the wafer stage is moved, and the other one-half 80 of the overlay metrology structure is exposed so that both exposed areas form a complete metrology structure (like KLA box in box).

[Para 29] The above-process may be repeated for the stage artifacts 72 and 74 in the other axis to form structures 82 and 84. The overlay structures are measured on a metrology tool. The measured overlay offsets are caused by grid placement errors, and calibration factors can be calculated and used for future wafers.

[Para 30] Figure 7 illustrates a third embodiment of the invention. With this embodiment, in addition to the interlocking boxes on product, the first level pattern also includes overlay metrology marks 86 and 90 that do not form a measurable overlay structure as the fields are stepped across the wafer 42. Before the wafer is removed from the chuck, the lithography tool is moved to one of the stage artifacts (shown in Figures 5 and 6), and the position of the artifact is measured using the tool"s alignment system. The lithography tool is moved a predetermined distance to the wafer, and the second part of an overlay metrology part on the wafer is exposed.

[Para 31] This procedure is repeated at each stage artifact position. Upon completion of wafer processing, the wafer is measured on the metrology tool. The metrology structures 60 and 62 formed as the fields were stepped on the wafer 20 are measured and analyzed for the difference between the field and grid parameters. The metrology structures 86 and 90 formed after movement from the stage artifact locations to the wafer locations are measured and analyzed to provide the grid parameters. From both sets of data, the field parameters can be mathematically obtained, and both field and grid offsets for future lots can be calculated.

[Para 32] The preferred embodiments of the invention, as discussed above in detail, have a number of advantages. For example, the invention allows grid terms to be measured independently of field terms, and when combined with the current practice, the invention allows the calculation of separate field errors and grid errors. In addition, the present invention does not require a separate photo level. Because of this, the invention reduces the cost of the product and, also, is not based on an assumption that the tool that laid down the photo, or zero, level, had no grid errors.

[Para 33] While it is apparent that the invention herein disclosed is well calculated to fulfill the objects previously stated, it will be appreciated that numerous modifications and embodiments may be devised by those skilled in the art, and it is intended that the appended claims cover all such modifications and embodiments as fall within the true spirit and scope of the present invention.